

## DESIGN AND ANALYSIS OF A SPARSE CHANNEL ADDER WITH HIGH PERFORMANCE AND ENERGY DELAY OPTIMIZATION

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### ABSTRACT

The design and analyzing of the sparse channel adder logic circuit with CSLA is proposed and processed in a Cadence 45nm CMOS. In order to overcome the limits than the existing adder the improvedSqrt-CSLA is proposed to reduce the delay process and also to improve the performances with efficient access. It is a parallel prefix form area of carry look ahead adder circuit.

It generates carry in  $(\log n)$  time and considered widely as the fastest adder and high performance arithmetic circuit in the industry. From the carries it computes fast by computing it in parallel at the increased area cost. The power analysis and delays are done and evaluate from the transient analysis.

**Keywords:** Adder, Carry-select-adder, Sparse-channels, Power-optimization

### I. INTRODUCTION

In recent years, many digital applications are scaled down the size of transistors. Cell phone, laptop, sensor, and other applications are disappeared in size over the last few decades. They are more portable to have chips in digital applications, in order to design and optimize

the transistors for better process in this case of pass transistor logic. It is an attractive solution for implementation of circuit of static CMOS with around half of the transistor in pass transistor logics [2], [3]. However it allows inputs to be tied with source and drain of transistors. It create possible situations to drive MOS has a logic 1 and PMOS has a logic 0. Since, NMOS is not a good for pull up device output of pass transistor circuit and suffer with a voltage drop  $V_{th}$ . It never achieves a full voltage swing to VDD with the supply of voltage in continuing scaling and this drop will not be tolerated [5-8].

In most of the technology the processors and adder are not used in the arithmetic logic unit, but other parts of the processor are used to calculate the addresses, table indices and similar application. The adders of other applications are in Multiply Accumulate structure, also used in high speed integrated circuit, in multiplier and execute various algorithms like FFT IIR and FIR in digital signal processing. Some of the substantial VLSI design areas are the low powers, area and high speed in logic circuit system of data path [1], [8]. On the requirement basis like areas delay and power consumption of the complex adders like Ripple Carry Adder, Carry look—Ahead Adder, Carry Select Adder and Ripple Carry—Adder (RCA). It shows the design compact with longer computation time and critical applications are derive for fast results by using CLA. But it leads to increase area and provides a compromise between the small areas. RCA

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provides with longer delay and for large area process with less delay of Carry Look Ahead adder [1], [11].

In this paper a proportional analysis of various adders and design of SQRT-CSLA is proposed and implemented for the better performance than the existing work. It process by Common Boolean Logic and the modified CSLA (MCSLA) is proposed by using Binary to Excess-1 (BEC) and modification CSLA is improved. In order to provide less area delay and power with better performance than the other adder [12-17].

The paper is organized in sections as follow: The related survey of adder and analysis the performance of the circuit with its limits in section II. The proposed circuit design and development of circuit flow work are described in Section III. The implementation and the proposed work procedure of improved SQRT - CSLA are presented in Section IV and in Section V the analysis of performances and the stimulation results are discussed. Finally in Section VI, the proposed work concludes with its performances and analysis, also with future work.

## II. LITERATURE SURVEY

In this section, the process of adder related to the logic circuit and the survey of the adder operation are discussed. For high performances of the execution cores in the logic and arithmetic logic unit the efficiency of energy is essential. For highest power density of the processor block is a part of the adder. It creates a thermal hot spots and sharp temperature gradients [1] to operate the system with the circuit which have high performance. The multiple ALUs presence in modern superscalar processors [3] and execution cores

of chip [5] further associate with aggravates the problem by impacting circuit reliability [10]. It increases the cooling costs for the purposes of design.

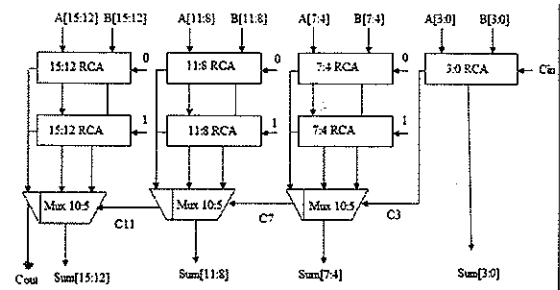


Fig.1: Carry Select Adder

At the same time, it critical the performances of the wide adders under different regions and appear of ALUs inside and microprocessor data path of FPUs [3]. Ripple Carry Adder have cascaded "N" single bit full adder and output carry of previous adder as input to next full adder carry. Therefore the worst case delay path of the adder carrier traverses the longest path through N stage. Fig [1] shows the ripple carry adder block diagram. The value of N increases the adder delay in a linear ways. Therefore the adder have a lowest speed of RCA with large propagation delay but least are only occupies in it. BEC uses less logic gates than the structure of N-bit full adder [9, 12-17].

In this paper, the basic idea is to implement Binary to Excess-1 converter (BEC) instead of RCA with conventional CSLA ( $C_{in}=1$ ) in order to provide less area and power. BEC required  $N+1$  bit by RCA need  $N$  bit [12]. Therefore in Modified CSLA process with less power and area than the conventional CSLA. SQRT-CSLA is selected for the comparison with modified design using BEC, as it has more balance in delay, low

power and less area [4]. The proposed modified SQR- CSLA uses dual RCAs, in order to decrease the same parameters. Fig [2] shows the 4 bit BEC with mux.

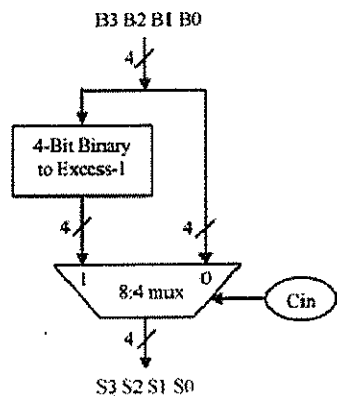


Fig. 2: 4 bit BEC with 8:4 mux

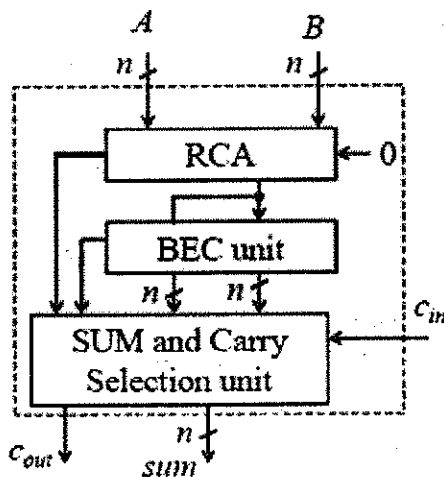


Fig.3: SQR-CSLA Circuit

**III. PROPOSED WORK**

In this section, the design and flow work of proposed adder circuits are processed in a Cadence 45nm CMOS are discussed. In the proposed design, by using Common Boolean Logic (CBL) sharing the improved SQR - CSLA circuit is proposed for better performance with less area, reducing delay and low power consumption than the

other adders or existing adder circuit from the modified SQR - CSLA. The SQR-CSLA based on CBL is shown in Fig [3].

The main idea of this work is to use BEC instead of RCA with carry  $C_{in}=1$  in order to moderate the area and power of conventional CSLA. BEC circuit is used to add the number 1 to the input. Circuit of BEC is shown in Fig [2]. The goal is achieved by using BEC with the multiplexer as shown in Fig [2]. One of the input of 8:4 MUX gets as its inputs (B3, B2, B1 and B0) and another input of MUX is BEC output. Boolean expressions of 4-bit BEC are as follow (Note: symbols ~NOT, &AND and ^XOR).

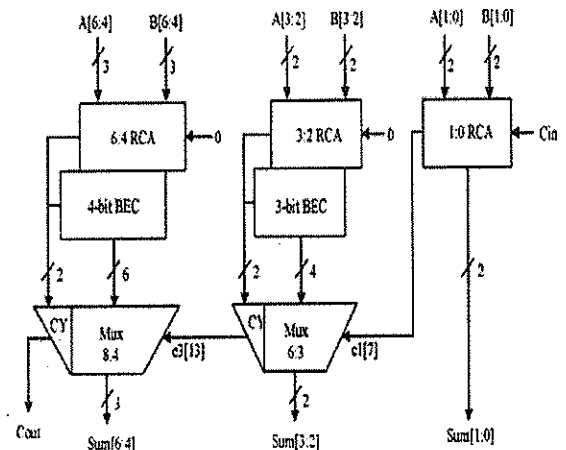


Fig.4: Improved SQR-CSLA Circuit

In design of binary full adder, the input of two 4 bit numbers A & B provides 4 bit Sum and carry elements as a output. Any adder form is added to any logic form of dynamic and static or with the variations or within families. In measuring optimized performance the factors like Area (A), Time (T). Power (P) or AT<sup>2</sup> are consider to evaluate the performance analysis, as well as flexible to optimize the design by anyone. The voltage swing in the noise margins should be at least 10%. In rise and fall

times, the input signals of the clocks less than 400 psec provides the output signals (10% to 90%) within 500 psec only. The load capacitance should have a 20 fF load for each output bit.

Based on the parameters the process of the design is done. In logic form, the proposed design is based on the static CMOS logic form. The low power consumption, Low sensitivity to noise, variations process and the fast speed are the properties in the inverter are consider for the evaluation and design process. The goal of the optimizations is to improve the speed and the performances of the adder. It is a speed—  
l i m i t i n g  
elements and optimized with the Time (T) factor. In the proposed design carry generation delay is evaluated to analysis the optimized process. Different optimized technics are considered to achieve the goal. The Logic-level optimization, Progressive Transistor Sizing, Transistor sizing, Layout Consideration and Transistor ordering are the process of optimization.

In Process technology and the kit design, CMOSISS design kit from Canadian Microelectronics Corporation (CMC) is selected and it is based on the Cadence 45nm CMOS process technology. In digital systems the logic circuits may be sequential or combinational. The logic gates are consists to determine the output time in the circuit form the combinational circuit performance with present input. The operations of the circuit are logically specified from the sequent of set of Boolean function. It employs the elements storage in the logic gate.

As per the procedure of logic design, in the circuit addition of 2 bit is perform in the combinational circuit as Half adder and with 3 bits as Full adder. In proposed design perform in hierarchical process of Full adder. As the procedure in the circuit the specification is defined to derive the truth table and the full adder is performed before the half adder. The simplified Boolean function is obtained from the table and performances of circuit and finally logic diagram is designed. The complete functions are identified by preprocessing, post processing and Carry look ahead network.

Preprocessing involves in computation and generates the propagate signals by the equation of logic ( $p_i = A_i \text{ xor } B_i$ ;  $g_i = A_i \text{ and } B_i$ ). Carry look ahead network differentiates the adder's performances and computes carries with corresponding bit, it groups the propagate and intermediate signals are generated by the logic equations ( $P_{i:j} = P_{i:k+1} \text{ and } P_{k:j}$ ;  $G_{i:j} = G_{i:k+1} \text{ or } (P_{i:k+1} \text{ and } G_{k:j})$ ). In post processing, all common adders involves computing of sum bit by the logic equation  $S_i = p_i \text{ xor } C_{i-1}$ .

#### IV. IMPLEMENTATION

In this section, the process of design implementation and generating block with bit propagate are presented. The schematic process of the bit propagates and generating blocks are evaluated and implemented. The blocks are generated with the logic ( $G_i = A_i \text{ AND } B_i$ ;  $P_i = A_i \text{ XOR } B_i$ ) and the schematic is shown in Fig [5].

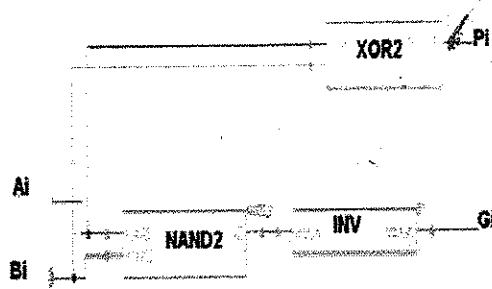


Fig.5: Schematic of Bit Propagate and Generate Block

a. Tri-state inverter design

The design of the adder with less transistor count adopt implementations of 3-module i.e. XOR (or XNOR). It requires at least 4 transistors for XOR (or XNOR) module implementation. But severe threshold voltage loss problems are faces in the design. The tri state inverter schematic diagram is shown in Fig [6]. The logic functions of the blocks are ( $G2 = G1 \text{ OR } (G0 \text{ AND } P1)$ ;  $P2 = P1 \text{ AND } P0$ ). The schematic diagram of the group generated block is shown in Fig [7].

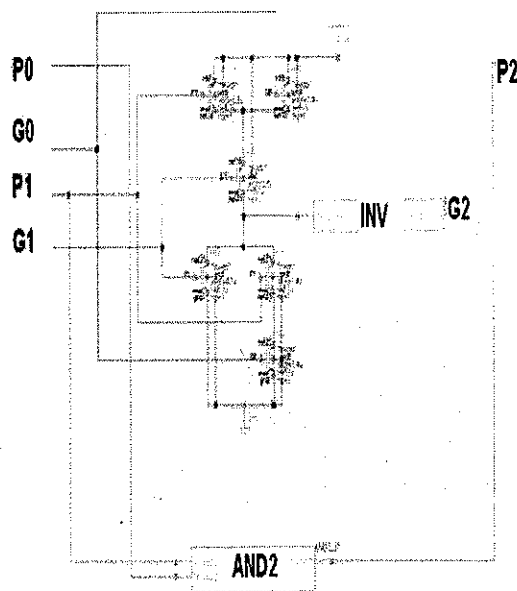


Fig.6 : Schematic of Group Propagate and Generate Block

The complete schematic diagram of the 8 bit is shown in Fig [8]. The color coding of the diagram shows that the Bit propagate and generate are indicate as white, Group propagate and generate are indicated as black, Group generate as grey and finally XOR as Half White Half Black.

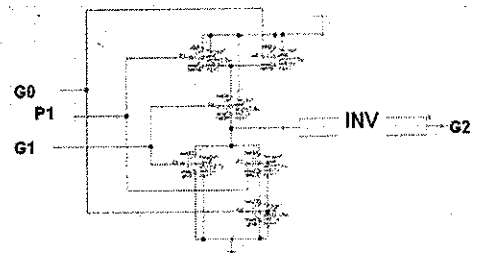


Fig.7: Schematic of Group Generate Block

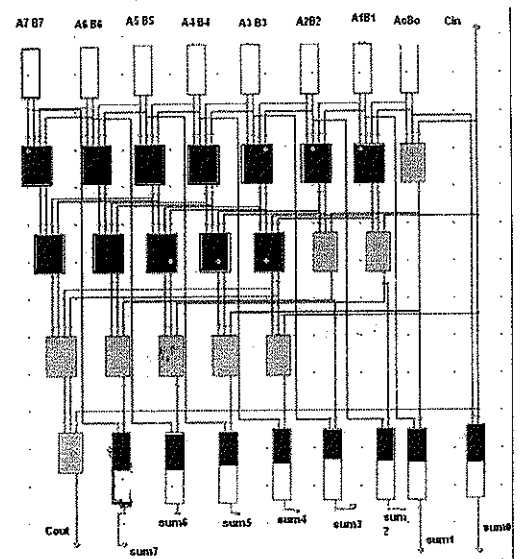


Fig.8: Complete schematic diagram of 8-bit

b. Layout

The layout of the circuit is design and process is done by using the technology Cadence Virtuoso Layout Editor Tool. The layout of the circuit implementation of majority gate is shown in Fig [9] and the runs of DRC and LVS are successfully done.

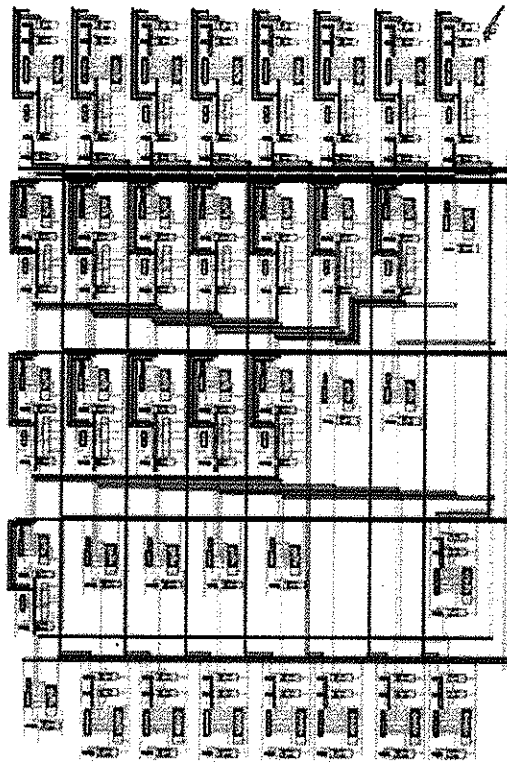


Fig.9: Complete Layout of 8-bit

c. 2-1 MUX

2-1 MUX is used as 2-input function in both sequential and combination logic circuit. The schematic implementation of a majority gate (A if S=0, and B if S=1). In other word, the output function is specified as  $(out = S^*A + S*B)$ . The logic function implementation is constructed as similar to majority gate described. The OR-AND logic expression is  $out' = (S+A^*)(S'+B')$ . In pull-down network the series is mapped with the transistors. Actually it achieves smallest area midstlogic styles and includesthe circuits of level-restorer than the implementation of logic. However, power consumption makes less attractive for low-power embedded applications.

V. SIMULATION RESULTS

The analysis of the circuit and the simulation results are evaluated in this section. The specification of the simulation process are Max frequency (374.94 MHz), Area(440  $\mu$  X 300 m = 0.132 mm<sup>2</sup>) and Power (460 uW). The inputs for the process are G (common input gate ofCMOS), P and N are input to the pMOS andnMOS source/drain).It randomly biased with a CMOS inverterat contrast. As shown in fig [10] the Worst case delay of the proposed circuit is obtained. In a CMOS logic circuit, either VDD or 0 is connected with the output through pull-up. PMOS are passing the VDD and NMOS and PMOS transistors are used in the pull-down and pull-up network.

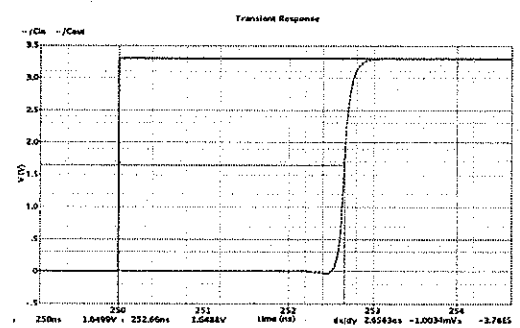


Fig.10: Transient analysis of the adder logic

The pass transistor logic circuit is does more work and transistor pass 0 and VDD than the CMOS logic circuit (only passes either 0 (NMOS) or VDD (PMOS)). Intuitively, in pass transistor logic circuit the transistor is required smaller than the CMOS logic circuit. So, full voltage swing is not achieved at output node because of pass 0 and VDD in pass transistor logic circuit. The transistor is passing one of 0 forvoltage

restoring output and restorer circuit level is affixed at the output node.

**A. Layout Consideration**

In circuit, based on the technology limits the ability of the transistors effectively is processed. Also some issues are there in it with F in FETs and independent mode of fins operating, by the input difficulty in it. However, inputs can be routed easily with fins, so the fins of PFInFET chosen to fins(3 fins to 1). Finally, Fin FET logic achieves an average reduction of 25% during implementation in cell area.

**B. Delay Extraction**

Delay is evaluated between 10% and 90% of voltage swing(0V to 1.2V), then the delay time for node A to go is also obtained from 0.1V to 0.99V. In the simulation process as an assumption the intermediate nodes have 1f F capacitance while 5f F capacitance applicable for input buses and output nodes. The circuit transient analysis is plotted as shown in Fig[10].

**C. Power Extraction**

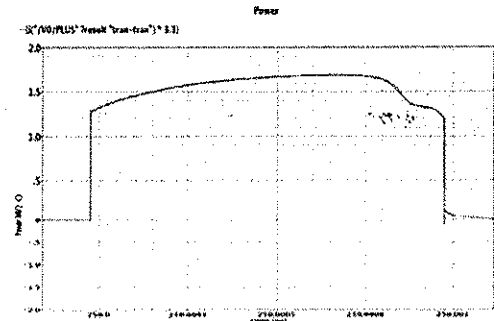
For the stimulation process dynamic power consumption is not considered on output node and input buses. In implementation of circuit for all nodes same time is considered for switches. In pass transistor logic implementation the sole exception is for majority gate. The comparison made for the circuit process between the inputs of 5 inputs (A, A', B, C, C') and 3 inputs (A', B', C') of the other circuit. By the lead of extra inputs more dynamic power consumption is take place in the pass transistor logic implementation. But highest active and leakage power consumption are already omitting dynamic power consumption calculation. As well as no

changes in usual inferior of power consumptions in pass transistor logic circuits.

The direct path of current from  $V_{DD}$  to ground is done by pull-up and pull-down active process, so the power consumed is as the active power. In this process leakage power is occur by transistor off when charges leak. The separate calculation of the power consumption components (active and leakage) is very difficult therefore the aggregated power consumption is evaluated by calculating instantaneous power first.

$$P(t) = V(t) * I(t)$$

Then all-time sum up P(t) to evaluate the operation total energy consumed. The analysis of power consumption is shown in Fig [11].



**Fig.11:Power Consumption of analysis**

Sentaurus provide information's about transistor voltage and current at any time. Finally the energy consumption is sum up for all transistors and by clock period it is divided to obtain the active and leakage power consumption, as listed in Table I for majority gate and 2-1 MUX functions. For consistency, least frequent switching input is placed closest to the output and near to supply rails the most frequent switching input is placed. Simulation results show that the logic circuits of pass transistor consume about 98% more power than

the existing logic circuit (consume least about 52% more power).

Table I: Performances analysis comparisons

Adder (Word Size 8 Bit)	Area (gate count)	Delay (ns)	Power (mW)	Power Delay Product (pWs)
Conventional (Dual RCA)	198	14.62	95.6	1366.36
Modified (with BEC)	154	16.52	85.32	1445.47
Regular SQRT (Dual RCA)	132	10.98	182	2300.56
Modified SQRT (with BEC)	128	12.25	175	2464.2

## VI. CONCLUSION

The delay power and area are the essential factors in VLSI design to show the performances of any circuit, as well as limits the performance of the circuit. The proposed work presents an approach to overcome the limits and issues of the existing system. It reduces the area delay and power and process with more power consumption and occupying more chip areas than the conventional carry select adder. The proposed structure of adder shows the performances with low powers, less delays and reduced areas than the structure of other adder. Also little bit faster than others and makes it simple and efficient for hardware implementation of VLSI

in a Cadence 45nm CMOS process using gpdk library functions.

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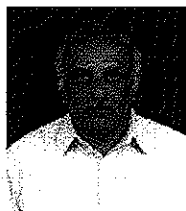
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